	Document ID	Pages	Title	Current OR	Current XRef	Inventor
1	US 6469343 B1	20	Multi-level type nonvolatile semiconductor memory device	257/324	257/295	Miura, Hirotomo et al.
2	US 4481527 A	8	High density MNOS transistor with ion implant into nitride layer adjacent gate electrode	257/325	257/326; 257/394; 257/395; 257/E29.309; 365/178; 365/184	Chen, Yung J et al.
3	US 6137718 A	6	Method for operating a non-volatile memory cell arrangement	365/185.03	257/324; 365/185.28	Reisinger, Hans
4	US 6011725 A	37	Two bit non volatile electrically erasable and programmable semiconductor memory cell utilizing asymmetrical charge trapping	365/185.33	257/E29.308; 365/131; 365/185.29	Eitan, Boaz

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	IS&R	L1	482	(257/324.326) CCLS.	USPAT US-PGPUB	2003/01/13 14:34
2	BRS	L2	41	1 and @pd>20020712	USPAT; US-PGPUB	2003/01/13 14:34
3	BRS	L5	8812	(multi adj bit) or mutlibit	USPAT; US-PGPUB	2003/01/13 14:54
4	BRS	L6	86	5 and mnos	USPAT; US-PGPUB	2003/01/13 15:03
5	BRS	L9	8	("5278440" | "5555204" | "5576564" | "5644528" | "5708285" | "5739528" | "6060723" | "6133603").PN.	USPAT	2003/01/13 14:53
6	BRS	L12	0	((multi adj bit) or mutlibit) and mnos	EPO; JPO; DERWENT; IBM_TDB	2003/01/13 14:56
7	BRS	L13	0	krick.in. or alberts.in.	IBM_TDB	2003/01/13 14:56
8	BRS	L14	2	earom adj cell	IBM_TDB	2003/01/13 14:58
9	BRS	L15	1	mnos adj fet adj memory adj array	IBM_TDB	2003/01/13 15:02
10	IS&R	L16	2	(("6137718") or ("6201282")).PN.	USPAT; US-PGPUB	2003/01/13 15:02
11	BRS	L17	1	6 and eitan.in.	USPAT; US-PGPUB	2003/01/13 15:05
12	IS&R	L18	1	("6030871").PN.	USPAT; US-PGPUB	2003/01/13 15:05

US-PAT-NO: 6414876

DOCUMENT-IDENTIFIER: US 6414876 B1

TITLE: Flash EEprom system

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Bulletin,
vol. 18, No. 12, May 1976, pp. 4192-4193.

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Bulletin, vol. 24, No. 7A, Dec. 1981, pp. 3311-3314, 4193.